

LH5332500B

CMOS 32M (4M × 8/2M × 16)
Mask-Programmable ROM

FEATURES

- 4,194,304 words × 8 bit organization (Byte mode)
2,097,152 words × 16 bit organization (Word mode)
- Access time: 150 ns (MAX.)
- Power consumption:
Operating: 357.5 mW (MAX.)
Standby: 550 μW (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
44-pin, 600-mil SOP
48-pin, 12 × 18 mm² TSOP (Type I)

DESCRIPTION

The LH5332500B is a 32M-bit mask-programmable ROM organized as 4,194,304 × 8 bits (Byte mode) or 2,097,152 × 16 bits (Word mode) that can be selected by a $\overline{\text{BYTE}}$ input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

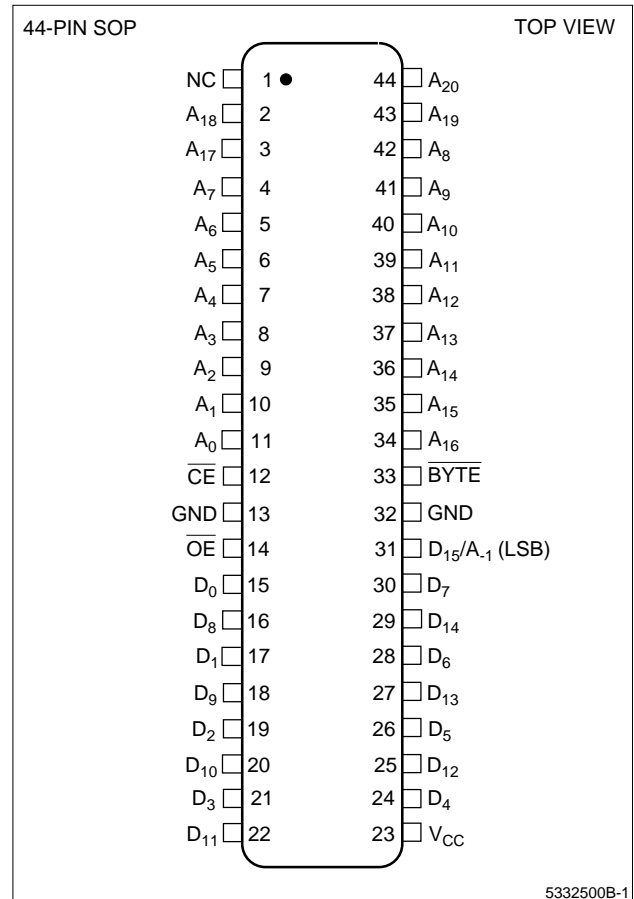


Figure 1. Pin Connections for SOP Package

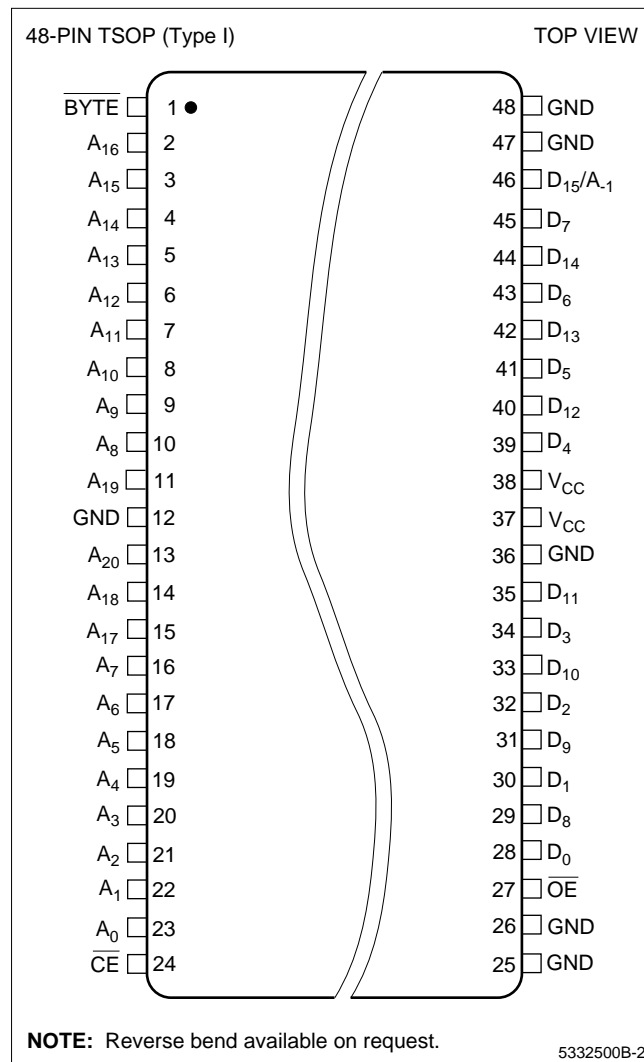


Figure 2. Pin Connections for TSOP Package

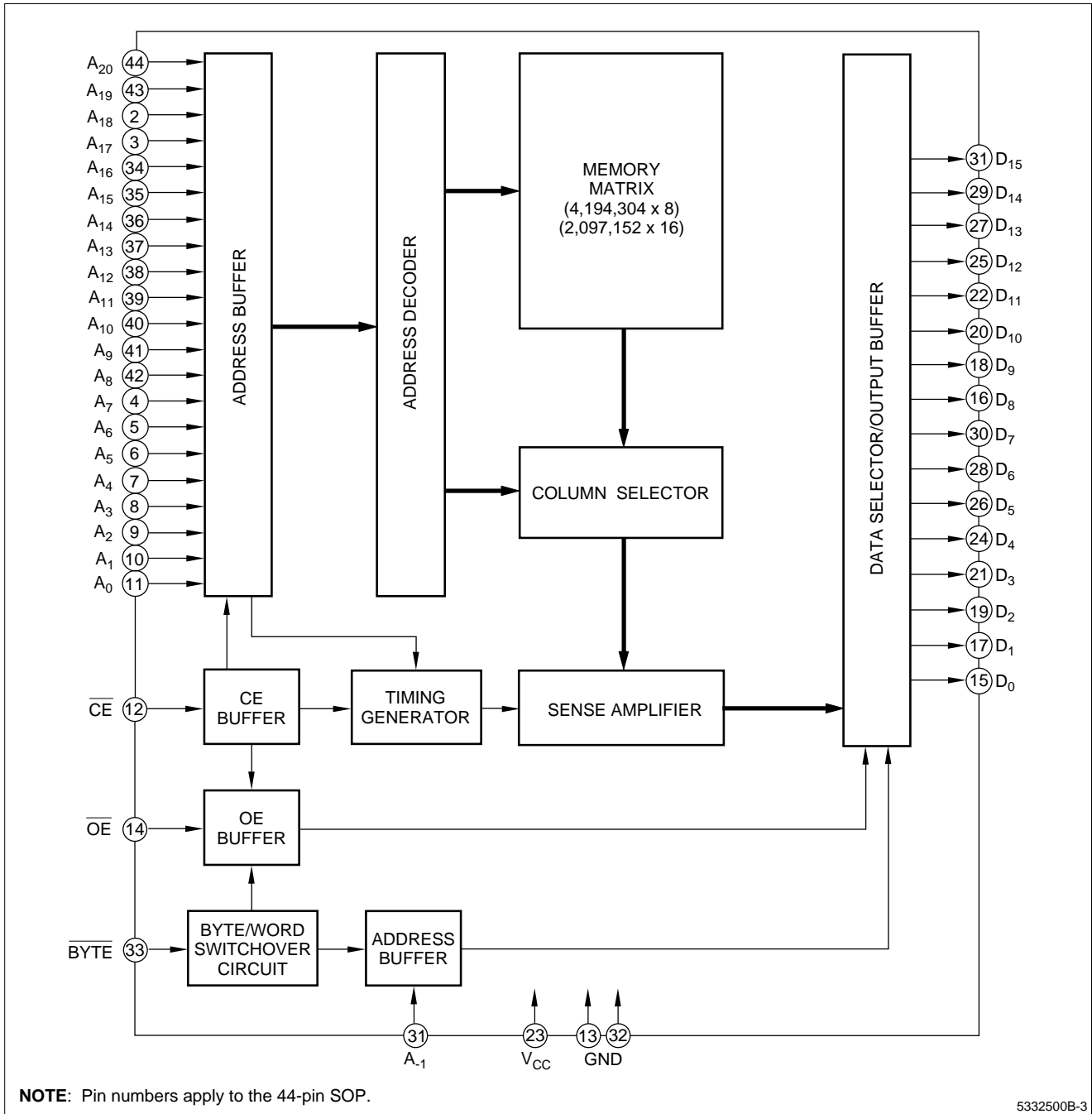


Figure 3. LH5332500B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A ₋₁ – A ₂₀	Address input	1
D ₀ – D ₁₅	Data output	1
$\overline{\text{BYTE}}$	Byte/word mode switch	1
$\overline{\text{CE}}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
$\overline{\text{OE}}$	Output Enable input	
V _{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. The D₁₅/A₋₁ pin becomes LSB address input (A₋₁) when the $\overline{\text{BYTE}}$ pin is set to be LOW in byte mode, and data output (D₁₅) when set to be HIGH in word mode.

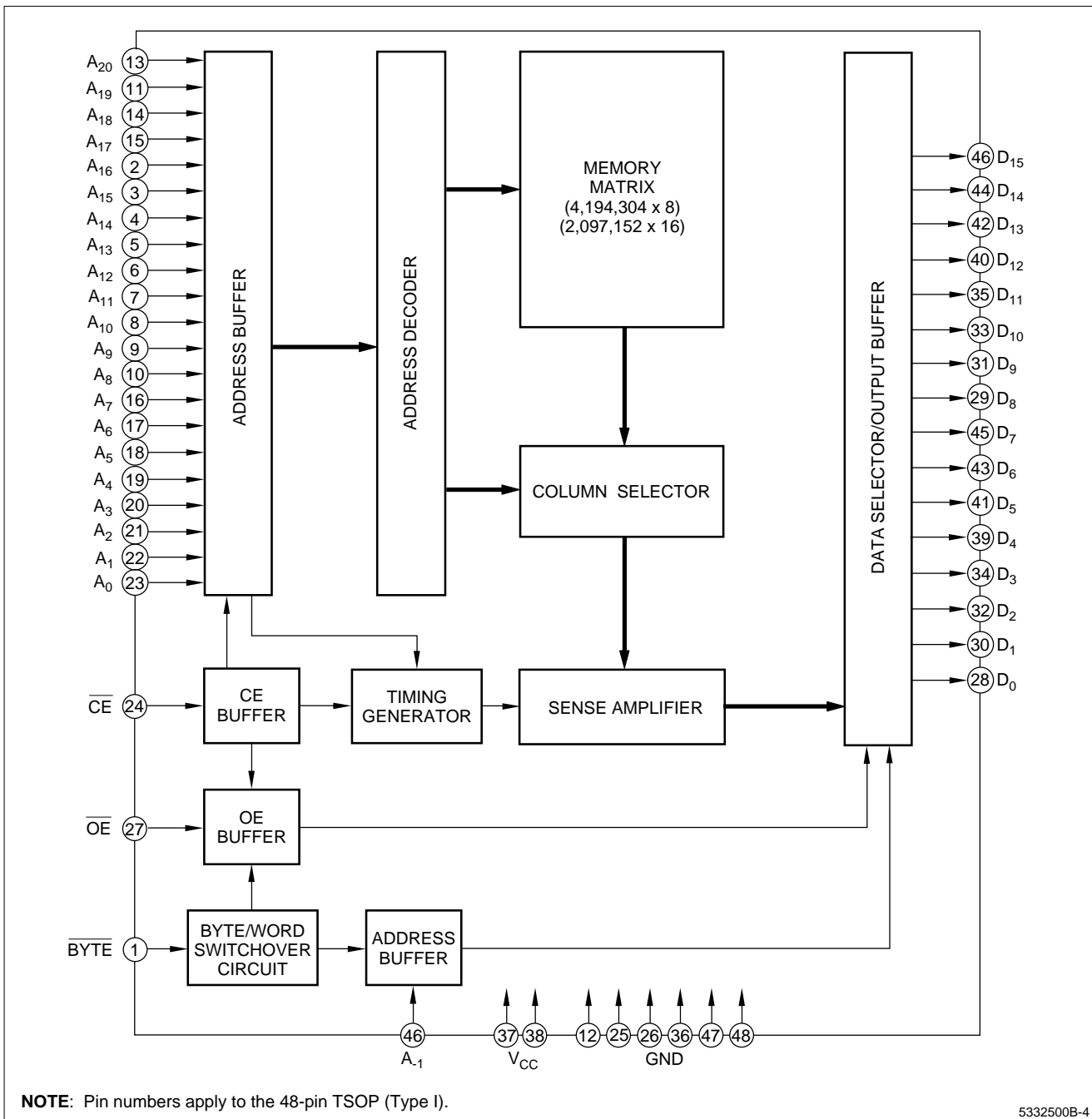


Figure 4. LH5332500B Block Diagram

TRUTH TABLE

\overline{CE}	\overline{OE}	BYTE	A-1 (D ₁₅)	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
				D ₀ - D ₇	D ₈ - D ₁₅	LSB	MSB	
H	X	X	X	High-Z	High-Z	–	–	Standby (I _{SB})
L	H	X	X	High-Z	High-Z	–	–	Operating (I _{CC})
L	L	H	–	D ₀ - D ₇	D ₈ - D ₁₅	A ₀	A ₂₀	Operating (I _{CC})
L	L	L	L	D ₀ - D ₇	High-Z	A ₋₁	A ₂₀	Operating (I _{CC})
L	L	L	H	D ₈ - D ₁₅	High-Z	A ₋₁	A ₂₀	Operating (I _{CC})

NOTE:

X = H or L; High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V _{CC}	-0.3 to +7.0	V
Input voltage	V _{IN}	-0.3 to V _{CC} + 0.3	V
Output voltage	V _{OUT}	-0.3 to V _{CC} + 0.3	V
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V _{IH}		2.2	V _{CC} + 0.3	V	
Input 'Low' voltage	V _{IL}		-0.3	0.8	V	
Output 'High' voltage	V _{OH}	I _{OH} = -400 μA	2.4		V	
Output 'Low' voltage	V _{OL}	I _{OL} = 2.0 mA		0.4	V	
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}		10	μA	
Output leakage current	I _{LO}	V _{OUT} = 0 V to V _{CC}		10	μA	1
Operating current	I _{CC1}	t _{RC} = 150 ns		65	mA	2
	I _{CC2}	t _{RC} = 1 μs		55	mA	2
Standby current	I _{SB1}	\overline{CE} = V _{IH}		2	mA	
	I _{SB2}	\overline{CE} = V _{CC} - 0.2 V		100	μA	
Input capacitance	C _{IN}	f = 1 MHz		10	pF	
Output capacitance	C _{OUT}	T _A = 25°C		10	pF	

NOTES:

1. $\overline{CE}/\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH} or V_{IL}, \overline{CE} = V_{IL}, outputs open

AC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0\text{ to }+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150		ns	
Address access time	t_{AA}		150	ns	
Chip enable access time	t_{ACE}		150	ns	
Output enable delay time	t_{OE}		70	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		60	ns	1
OE to output in High-Z	t_{OHZ}		60	ns	

NOTE:

1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 V to 2.6 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL + 100 pF

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

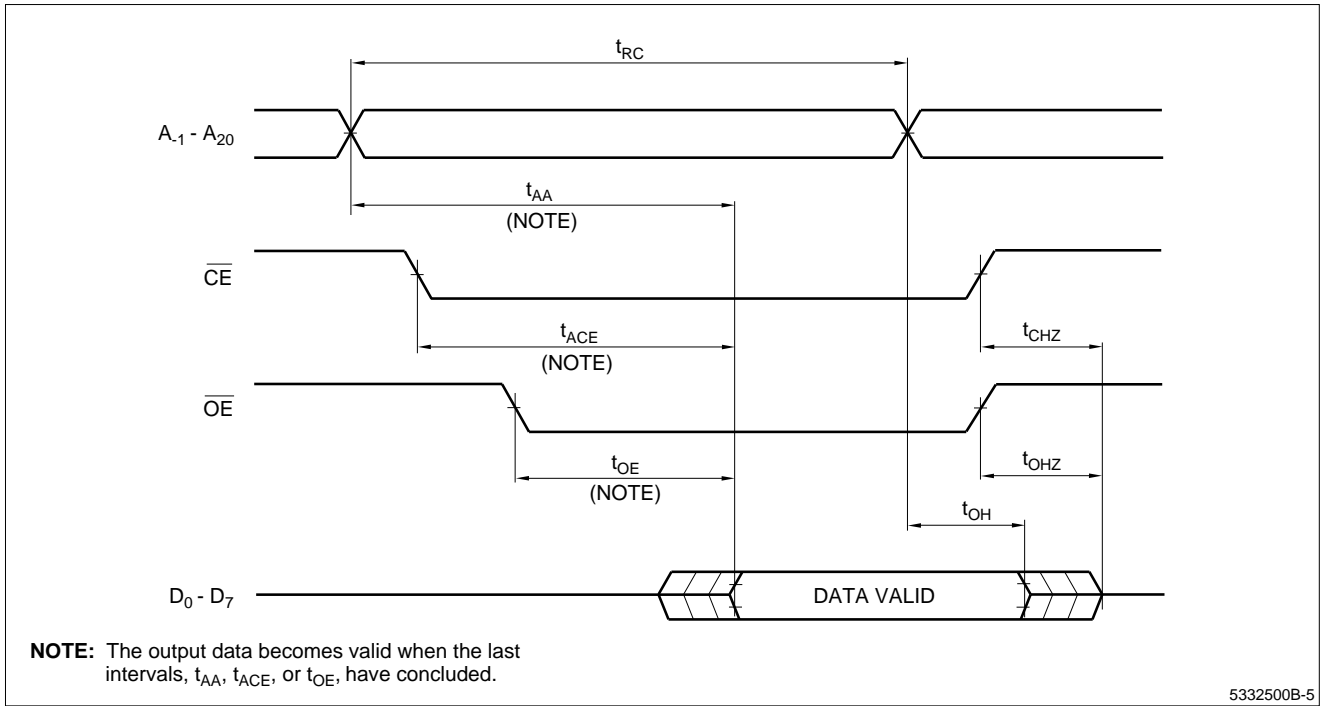


Figure 5. Byte Mode ($\overline{BYTE} = V_{IL}$)

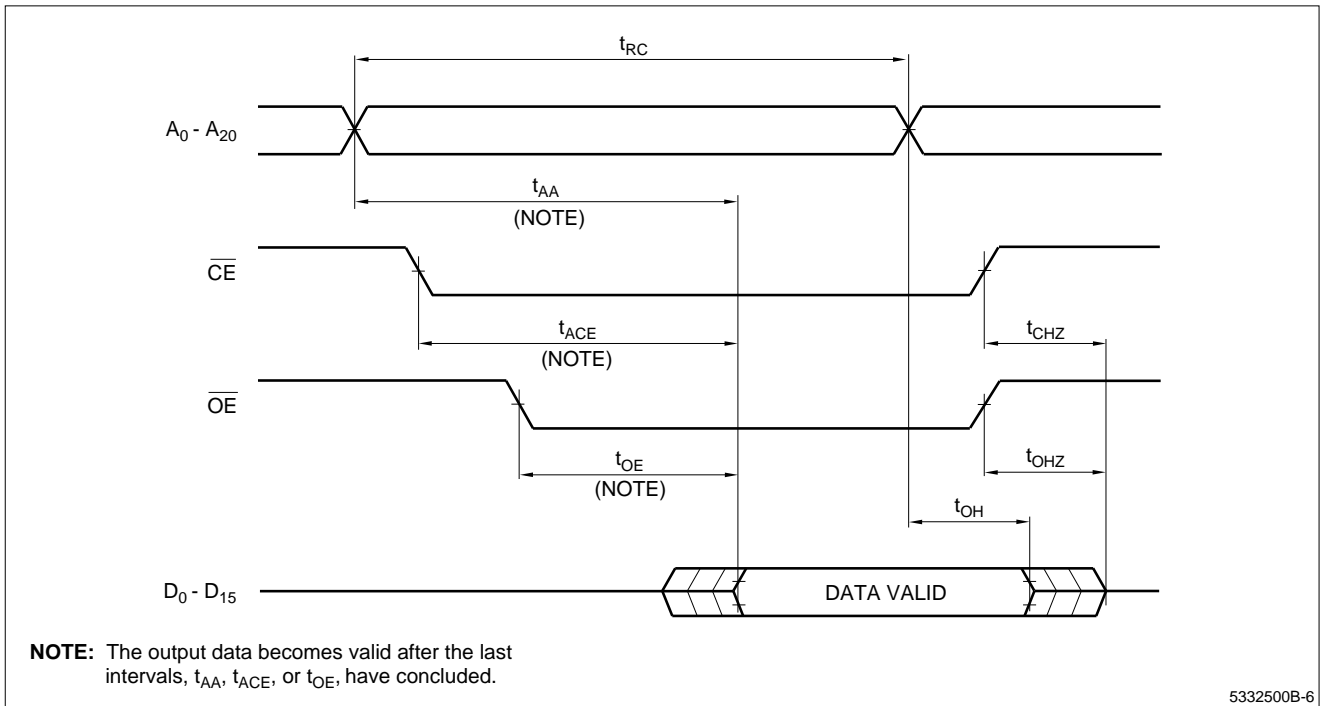
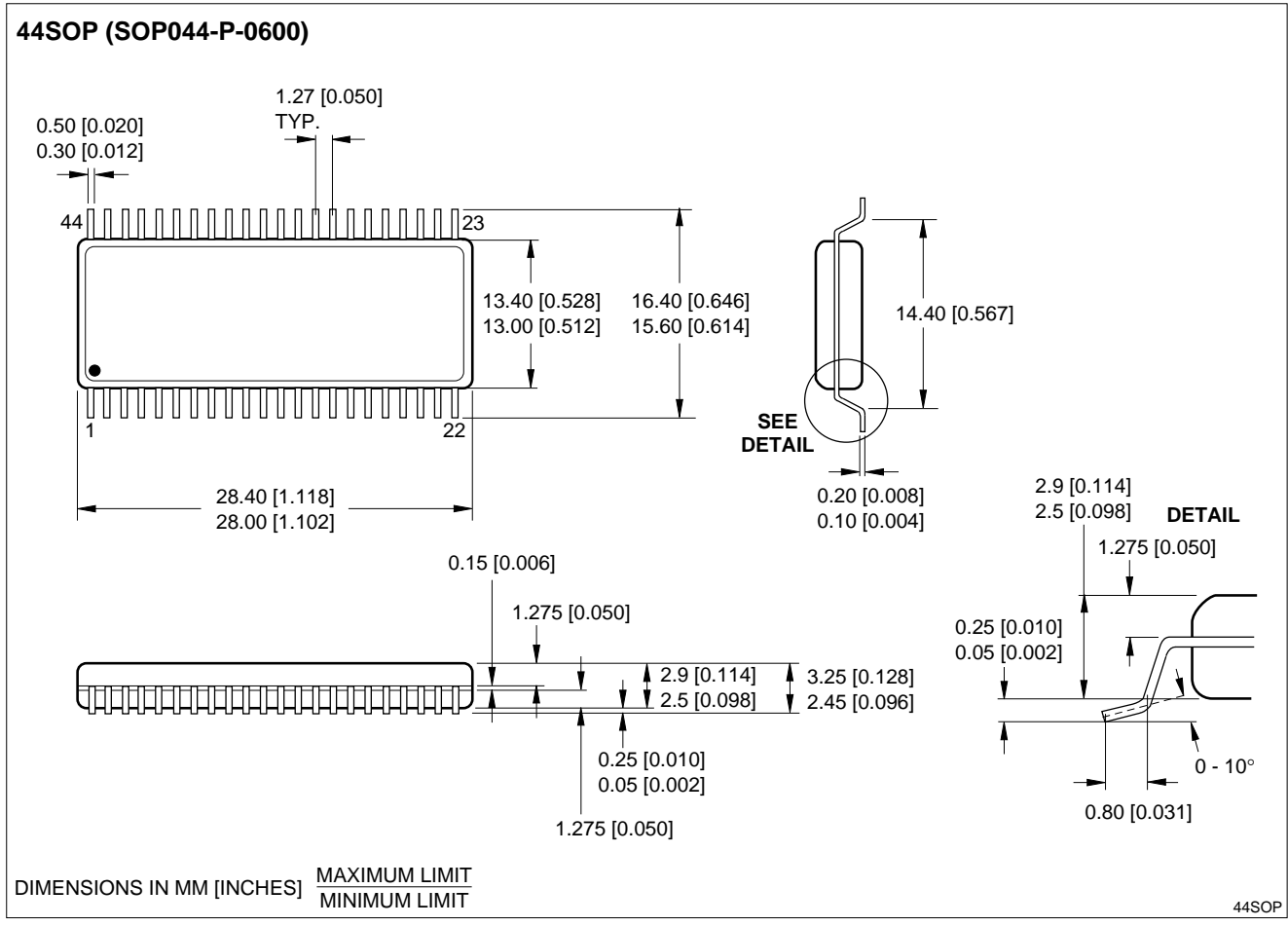
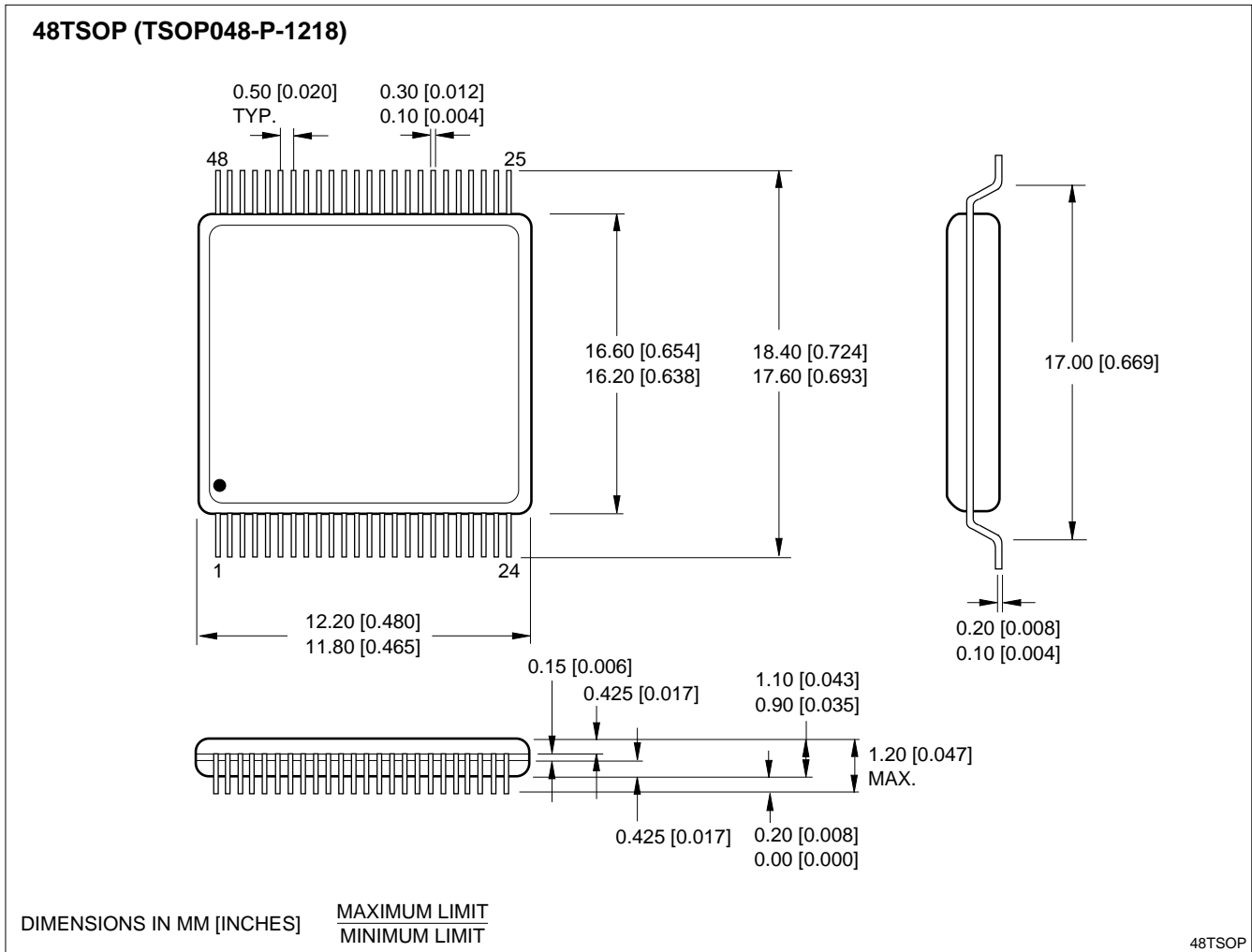


Figure 6. Word Mode ($\overline{BYTE} = V_{IH}$)

PACKAGE DIAGRAMS



44-pin, 600-mil SOP



48-pin, 12 × 18 mm² TSOP (Type I)

ORDERING INFORMATION

